UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,034	12/09/2003	Wolfgang Siebert	SIEBERT ET AL - 2 (DIV)	6746

7590 03/09/2005

Collard & Roe, P.C.
1077 Northern Boulevard
Roslyn, NY 11576

EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,034	SIEBERT ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6 and 8-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6, 8-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 2/18/05 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 6,630,024 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-6, 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujikawa et al. (US 6,261,362 of record) in view of Sakata et al. (EP 0711854 cited by applicants) and Liaw et al. (reference AT cited by applicants).

Fujikawa teaches a process for producing a semiconductor wafer with a front surface and a back surface and an epitaxial layer of semiconducting material deposited on the front surface, wherein the process comprises the following process steps:

(a) a stock removal step comprises grinding the surface of the wafer, mirror polishing one side or both sides of the wafer, finish polishing and washing the wafer (col. 6, lines 36-43 and Embodiment 2);

(b) pretreating of the front surface of the semiconductor wafer at a temperature of 1150 degrees Celsius in an epitaxy reactor; and

(c) depositing of the epitaxial layer on the front surface of the pretreated semiconductor wafer.

Fujikawa differs from the claims in that while Fujikawa prepares the semiconductor wafer for subsequent epitaxial deposition using conventional stock removal process consists of two or three polishing steps, the claims call for a stock removal process consists of only one polishing step.

Sakata teaches a method for the preparation of a mirror-polished semiconductor wafer in which the wafer is subjected to a stock removal polishing step as the only polishing step to produce a mirror-polished wafer which is, after washing and drying, subjected to an epitaxial deposition of silicon on the mirror-polished surface. The single step polishing method of Sakata results in the mirror-polished wafer having the same excellent quality as prepared by conventional process, which utilizes two or three polishing steps, while increases productivity and reduces manufacturing cost by the omission of subsequent polishing steps (col. 2, lines 11-19; col. 4, lines 20-33 and 42-57; col. 6, lines 15-35; col. 12, lines 16-33.)

The subject matter as a whole would have been obvious to one of ordinary skill in the art to modify the process of Fujikawa by performing the above step a) using the process taught by Sakata because of the foregoing

benefits. That is, by the omission of subsequent polishing steps, productivity is improved and production cost is reduced.

The combined process of Fujikawa and Sakata now differs from the claims in not disclosing the amount of material removed from the surface of the semiconductor wafer in the above pretreating step (b) even though Fujikawa teaches the pretreating is performed in H2+HCl ambient at 1150°C for 100 seconds (see Fig. 5).

Liaw teaches a pretreating process of a semiconductor substrate in which an in-situ HCl etching and H2 prebake process is performed on the surface of the substrate to remove 0.1- 0.5 μm of material from the surface. The amount of material removed results in a very clean and damage free surfaces which has been very effective for the elimination of epitaxial stacking faults and spikes (see section 1.8.3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of the combination by removing 0.1- 0.5 μm of material from the surface of the semiconductor wafer in the pretreating step (b) because this would produces a damage-free surfaces of the wafer, which would eliminate stacking faults and spikes in the epitaxial layer deposited in step (c). Note that in the pretreating step in H2+HCl for 100 seconds to remove 0.1- 0.5 μm of material, the etching rate must be in a range of 0.06 to 0.3 μm/min which overlaps the range as claimed.

For the limitation regarding to the claimed cleaning and drying, see col. 4, line 55 in Sakata.

For claim 5, see Fig. 5 in Fujikawa, which depicts a wafer pre-processing step immediately before the epitaxial deposition.

For claim 6, see Fig. 5 in Fujikawa, which depicts a wafer pre-processing step in an atmosphere containing hydrogen at a temperature of 1150 °C.

For claim 8, Fig. 5 in Fujikawa shows the epitaxial layer deposited has a thickness of 4 microns.

For claim 11, see Fujikawa, col. 1, lines 5-9.

3. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujikawa et al. taken with Sakata et al. and Liaw et al. as applied to claims 2-6, 8 and 11 above, and further in view of Fabry et al. (US 5,219,613 of record).

The combination Fujikawa et al., Sakata et al., and Liaw et al. teaches the claimed invention as described above except for the claimed rendering hydrophilic of the deposited epitaxial layer using an oxidizing gas (claim 9) or wet-chemical means (claim 10).

Fabry teaches a method in which the surface of a silicon wafer is rendered hydrophilic by exposing the wafer in an oxidizing gas (col. 2, lines 52-56) and subsequently exposing the oxidized wafer in a solution of organosilicon compound (col. 3, lines 4-10; col. 3, lines 60-61 and claim 7). Note that the surface of the oxidized wafer has hydrophilic property (col. 6, lines 1-3).

The subject matter as a whole would have been obvious to one of ordinary skill in the art to modify the combined process of Fujikawa and

Sakata by rendering the surface of the epitaxial silicon layer according to the process taught by Fabry because the wafer treated in such a manner has a high storage stability, hence preserving its surface nature during a long storage period before the wafer is used for the fabrication semiconductor devices on the epitaxial layer.

Response to Arguments

4. Applicant's arguments with respect to claim 2 have been considered but are moot in view of the new ground(s) of rejection.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on

access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

03/07/05